IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : **Confirmation No. 5201**

Syuji MATSUDA et al. : Attorney Docket No. 2004_1091A

Serial No. 10/501,150

Filed July 13, 2004

INTERLEAVED DATA ERROR CORRECTION METHOD DEVICE

PATENT OFFICE FEE TRANSMITTAL FORM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is a check in the amount of $130.00 to cover Patent Office fees relating to filing the following attached papers:

Petition to Make Special $130.00

A duplicate copy of this paper is being submitted for use in the Accounting Division, Office of Finance.

The Commissioner is authorized to charge any deficiency or to credit any overpayment associated with this communication to Deposit Account No. 23-0975, with the EXCEPTION of deficiencies in fees for multiple dependent claims in new applications.

Respectfully submitted,

Syuji MATSUDA et al.

THE COMMISSIONER IS AUTHORIZED TO CHARGE ANY DEFICIENCY IN THE FEES FOR THIS PAPER TO DEPOSIT ACCOUNT NO. 23-0975

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	**Mail Stop: PETITION BRANCH**
Syuji MATSUDA et al.	:	**Confirmation No. 5201**
Serial No. 10/501,150	:	Attorney Docket No. 2004_1091A
Filed July 13, 2004	:	Group Art Unit 2113

INTERLEAVED DATA ERROR CORRECTION METHOD DEVICE

PETITION TO MAKE SPECIAL
REQUEST FOR ACCELERATED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Petition is hereby made to make the above identified application special and accelerate examination of this application. As per the requirements of MPEP 708.02, section VIII, the Applicants provide each of the required items **(A)-(E)** as follows:

(A) Accompanied with this petition to make special is the required fee set forth in 37 C.F.R. 1.17(h);

(B) A Preliminary Amendment was submitted on July 7, 2006 which added new claims 17-40. Applicants submit that all of the claims (i.e., claims 1-40) of this application are directed to a single invention, but in the event that the Patent Office takes the position that all the claims presented are not obviously directed to a single invention, Applicants hereby offer to make an election without traverse;

(C) Applicants submit that a pre-examination search was made. As the basis for the pre-examination search, Applicants rely on the search made by the Japanese Patent Office in the International Search Report for International Application No. PCT/JP03/06909, of which the present application is the National Stage application. The International Search Report was submitted in the present application with an IDS on September 20, 2004. Applicants note that the claims in the international application are of a similar scope to the claims in the present application.

(D) Applicants submit that the following are the references deemed most closely related to the subject matter encompassed by the claims:

I. JP 07-123013; and

II. JP 2002-521789 (corresponds to WO 00/07300).

Applicants note that each of the above-noted references was submitted along with the Information Disclosure Statement filed in the present application on September 20, 2004.

(E) Applicants provide the following detailed discussion of the above-mentioned references which points out how the claimed subject matter of the present application is patentable over the references:

Detailed Discussion

The present application includes claims 1-40, of which claims 1, 7, 17, 22, 27 and 32 are independent claims. These claims recite at least the following features that Applicants submit are not anticipated, suggested, or rendered obvious by the references listed in section (D) above:

Claim 1 recites the features of a judgement step of, with a code line to be subjected to error correction being in a target code line, judging whether or not the position of a target byte in the target code line is on the boundary with a data region which comprise error correction codes that are independent from error correction codes in said target code line, with the erasure position

information which is used when performing error correction on a code line that is previous to the target code line in the error correction order, and judging, according to the result of judgement, as to which erasure position information to be used for tracking down an error in the target block, the erasure position information in the target code line or the erasure position information which is used when performing error correction on the code line that is previous to the target code line in the error correction order.

Claim 7 recites the features of a comparator for comparing an erasure position information of the target code line with the erasure position information which has been used when performing error correction on a code line that is previous to the target code line in the error correction order and is stored in the storage unit; wherein an error correction circuit performs error correction on the target code line, according to the result of the comparison by the comparator, using, as the erasure position information for tracking down an error in the target code line, the parameter of the target code line or the erasure position information which has been used when performing error correction on a code line that is previous to the target code line in the error correction order.

Claim 17 recites the features of judging whether or not a first data, which is one of the elements of code line in an error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved; and configuring erasure position information of the second data as erasure position information of the first data when the first and second data existed between the same sub data.

Claim 22 recites the features of judging whether or not a first data, which is one of the elements of code line in an error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction by using the erasure position information; and configuring erasure position information of second data as erasure position information of the first data when the judgment step judges the first and second data existed between the same sub data, and

configuring every element of code line in the error correction target when the code line of the previous error correction performed error correction without using erasure position information.

Claim 27 recites the features of a judgment means for judging whether or not a first data, which is one of the elements of code line in the error correction target, and a second data, which exist on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved; and a configuration means for configuring erasure position information of the second data as erasure position information of the first data when the first and second data existed between the same sub data.

Claim 32 recites the features of a judgment means for judging whether or not a first data, which is one of the elements of code line in an error correction target, and a second data, which exists on the same position as the first data in the code line of previous error correction, existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction by using the erasure position information; and a configuration means for configuring erasure position information of the second data as erasure position information of the first data when the judgment step judges the first and second data existed between the same sub data, and configuring every element of code line in the error correction target when the code line of the previous error correction performed error correction without using erasure position information.

Applicants submit that at least the above features recited in independent claims 1, 7, 17, 22, 27 and 32 are not anticipated, suggested or rendered obvious by the references listed in section (D) above, for the following reasons:

I. JP 07-123013

This reference discloses a device for performing error correction using double Reed-Solomon codes having C1 series and C2 series (see Abstract). Blocks of the C2 series are grouped into sub groups, in each of which words of the C2 series are in duplicate with words of the C1 series (see Abstract). A C1 error flag is read from designated blocks and evaluated, its error location and error numbers to be counted are stored, but the C1 error is not read from other blocks, and in the other mode, whether correction of the series C2 is executed depends on the

value of the C1 flag in erroneous data based on the location of erroneous data of the C2 series (see Abstract).

Thus, while this reference discloses an error correction device utilizing double Reed-Solomon codes comprising C1 series and C2 series, in which the correction of the series C2 depends on the value of the C1 flag in erroneous data based on the location of erroneous data of the C2 series, Applicants respectfully submit that this reference does not disclose or suggest at least the above-noted features recited in claims 1, 7, 17, 22, 27 and 32 regarding the erasure position information that is used when performing error correction on a code line that is previous to a target code line in a correction order, the ability to judge whether or not first and second data existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction using the erasure position information, and configuring the erasure position information.

II. JP 2002-521789 (corresponds to WO 00/07300))

This reference discloses an error correction method which allows clue words to cooperate with synchronizing bit groups in a systematic format, in which clues originate in both high protectivity clue words interleaved among clue columns, and in synchronizing columns constituted from synchronizing bit groups (see WO 00/07300 at page 1, lines 17-18, Abstract, and page 14, lines 3-8).

Thus, while this reference discloses an error correction method which utilizes clues that are interleaved among clue columns, and clues that originate in synchronizing columns, Applicants respectfully submit that this reference does not disclose or suggest at least the above-noted features recited in claims 1, 7, 17, 22, 27 and 32 regarding the erasure position information that is used when performing error correction on a code line that is previous to a target code line in a correction order, the ability to judge whether or not first and second data existed between the same sub data before being deinterleaved when the code line of the previous error correction performed error correction using the erasure position information, and configuring the erasure position information.

Conclusion

Because of the above mentioned distinctions, Applicants submit that independent claims 1, 7, 17, 22, 27 and 32, and all claims that depend therefrom, are not anticipated by any of the above mentioned references. Further, Applicants submit that the distinctions are such that a person having ordinary skill in the art at the time of the invention would not have been motivated to modify or combine any of the above mentioned references in such a manner so as to result in, or otherwise render obvious, the present invention as recited in claims 1-40. Therefore, Applicants submit that claims 1-40 are allowable over the above mentioned prior art references.

In view of the forgoing, since Applicants have provided each of the necessary items (A)-(E) identified above, Applicants respectfully request that this Petition to Make Special be granted and the examination of this application be accelerated.

The Special Program Examiner is invited to contact the undersigned by telephone if it is felt that there are any issues remaining which must be resolved before the granting of this Petition to Make Special.

Moreover, for at least the reasons found in item (E) above, it is submitted that the present application is clearly allowable over the prior art of record.

In the event, however, that the Examiner has any comments or suggestions of a nature necessary to place this case in condition for allowance, then the Examiner is kindly requested to contact Applicants' undersigned attorney by telephone to promptly resolve any such matters.

Respectfully submitted,

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